REMARKS

Reconsideration of this application as amended is respectfully requested. Claims 16, 25, 31 and 33 have been canceled without prejudice, and claims 15, 17, 24, 26, 34 and 35 have been amended without adding new matter. Claims 1-15 and 17-24, 26-30 and 32-35 remain pending. The remarks below in connection with claim rejections refer to the claims as amended herein.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 2, 14-17, 24-26 and 33 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,121,791 to Abbot ("Abbot").

Claims 16, 25 and 33 have been canceled, rendering rejection of those claims moot.

Applicant submits that the rejection of claim 26 is also moot as the limitations of claim 31 have been incorporated into independent claim 26 in accordance with the suggestion for allowability set forth in the Office Action; effectively rewriting claim 31 in independent form to include the limitations of base claim 26 and any intervening claims.

Applicant submits that the remaining rejected claims, 1, 2, 14, 15, 17 and 24, are not anticipated by Abbot at least for the reasons set forth below.

Claim 1 recites, in part:

> switch circuitry coupled to receive input data, the switch circuitry coupled to the control logic to receive a result of the AB logic operation from each of the plurality of logic cells and selectively enable the output of one or more bits of the input data based on the result of the AB logic operation

Abbot discloses a field programmable device having a programmable logic data path to perform logic operations (Abbot, col. 4, line 50 – col. 5, line 22) and more specifically that the logic data path includes a rearrangement circuit 202 to allow for flexible rearrangement and duplication of input data bits (Abbot, col. 6, lines 40-42). Assuming arguendo that the rearrangement circuit of Abbot corresponds to the switch circuitry of claim 1 as posited in the Office Action, Abbot still does not disclose or suggest that the rearrangement circuit is "coupled to receive a result of the AB logic operation from each of the plurality of logic cells and

selectively enable the output of one or more bits of the input data based on the result of the AB logic operation" as recited in claim 1, nor has any such disclosure or suggestion been pointed out in the Office Action[1]. Accordingly, Abbot lacks at least the above-recited limitation and therefore does not anticipate claim 1, nor dependent claims 2 and 14.

Claim 15 recites, in part:

> performing an AB logic operation in each of the logic cells;
>
> selecting among a second one or more bits of input data using a result of the AB logic operation in at least one of the logic cells; and
>
> selecting between the selected second one or more bits of input data and a first one or more bits of input data for output to a comparand in the CAM device

Applicant submits that, for at least the reasons given with respect to claim 1, Abbot does not disclose or suggest the above-recited combination and therefore does not anticipate claim 15, nor dependent claim 17.

Claim 24 recites, in part:

> means for performing an AB logic operation in each of the logic cells;
>
> means for selecting among a second one or more bits of input data using a result of the AB logic operation in at least one of the logic cells; and
>
> means for selecting between the selected second one or more bits of input data and a first one or more bits of input data for output to a comparand in the CAM device

Applicant submits that, for at least the reasons given with respect to claim 1, Abbot does not disclose or suggest the above-recited combination and therefore does not anticipate claim 24.

Allowable Subject Matter

Claims 3-13, 18-23, 27-32, 34 and 35 have been objected to as being dependent upon a

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1 Applicant notes, for example, that the portion of Abbot referenced in the Office Action (Abbot col. 7, lines 30-35) merely provides that rearrangement circuit 202 is followed by a selective field negation circuit 210 that selectively negates certain bits output by the rearrangement circuit based on control bits provided by a decoding logic unit.

rejected base claim, but indicated to be allowable if rewritten in independent form to include all the limitations of their respective base claims and any intervening claims. Applicant has amended claims 34 and 35 in accordance with the suggestion for allowability and respectfully submits that the objection to those claims is overcome. As discussed, applicant has also effectively followed the suggestion for allowability of claim 31 by incorporating the limitations of claim 31 into independent claim 26 from which claim 31 directly depends.

In view of the foregoing remarks regarding independent claims 1, 15 and 26, applicant respectfully declines to amend claims 3-13, 18-23 and 27-30 and 32 at this time.

In Conclusion

Applicant respectfully submits that all pending claims are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

If an extension of time is due in connection herewith, applicant hereby petitions for such extension of time.

Authorization is hereby given to charge deposit account 501914 for any fee due in connection with this submission, including any extension-of-time fee.

Respectfully submitted,

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Dated: March 12, 2007 By: 

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